UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/827,045	04/19/2004	Trudy L. Benjamin	200311485-1	2390

22879 7590 05/02/2006

HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER	
MARTIN, LAURA E	

ART UNIT	PAPER NUMBER
2853	

DATE MAILED: 05/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/827,045	BENJAMIN ET AL.	
	Examiner	Art Unit	
	Laura E. Martin	2853	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/19/04, 11/9/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 4-8, 10-18, 24-26, 33-44 are rejected under 35 U.S.C. 102(b) as being anticipated by Axtell et al. (US 20020093551).

As per claim 1, Axtell et al. teaches a fluid ejection device comprising: a fire line (figure 6, element FIRE) configured to receive an energy signal having energy pulses; a drive switch (figure 7, element 101) configured to control the energy signal to eject fluid; a first transistor having a first gate (figure 6, element 111) configured in a first loop structure; a second transistor having a second gate configured in a second loop structure (figure 7, element 113); and a third transistor having a third gate configured in a third loop (figure 7, element 115) structure disposed around the first transistor, wherein the second transistor and the third transistor share a first active region, and wherein the first transistor and at least one of the second and third transistors are configured to control the drive switch [0074].

As per claim 2, Axtell et al. teaches a fluid ejection device, wherein the second transistor and the third transistor are configured to control the drive switch [0074].

As per claim 4, Axtell et al. teaches a fluid ejection device, comprising: a fourth transistor having a fourth gate configured in a fourth loop structure (figure 7, element 105), wherein the second transistor and the fourth transistor share a second active region and the first gate is disposed around a third active region that is electrically coupled to the second active region.

As per claim 5, Axtell et al. teaches a fluid ejection device, wherein the fourth gate is disposed around a fourth active region (figure 7, element 105) that is configured to receive a signal to charge the second active region and the third active region (figure 7, element 113 and 115).

As per claim 6, Axtell et al. teaches a fluid ejection device, comprising: a fourth transistor having a fourth gate configured in a fourth loop structure (figure 7, element 107), wherein the second transistor and the fourth transistor share a second active region (figure 7, elements 113 and 115).

As per claim 7, Axtell et al. teaches a fluid ejection device, wherein the fourth gate is disposed around a third active region and the first gate is disposed around a fourth active region that is electrically coupled to the third active region (figure 7, elements 107 and 111).

As per claim 8, Axtell et al. teaches a fluid ejection device, wherein the second active region is configured to receive a signal to charge the third active region and the fourth active region [0074-0076].

As per claim 10, Axtell et al. teaches a fluid ejection device, wherein the third gate is disposed (figure 7, element 113) around the second transistor.

As per claim 11, Axtell et al. teaches a fluid ejection device, wherein the third gate is disposed around the second transistor (figure 7, element 113) and the first gate is within the second gate (figure 7, elements 111 and 113).

As per claim 12, Axtell et al. teaches a fluid ejection device, wherein the second gate is disposed around the third transistor (figure 7, elements 113 and 115).

As per claim 13, Axtell et al. teaches a fluid ejection device, wherein the first transistor and the second transistor share the first active region (figure 7, elements 111 and 113).

As per claim 14, Axtell et al. teaches a fluid ejection device, wherein the first transistor and the second transistor share the first active region (figure 7, elements 111 and 113) and the first gate is disposed around a second active region that is configured to receive a signal to charge the first active region.

As per claim 15, Axtell et al. teaches a fluid ejection device, wherein the second gate (figure 3, element 113) is disposed around a third active region that is coupled to date/address transistors (figure 7, 111 and 115) and the first active region is coupled to the drive switch (figure 7, element 101).

As per claim 16, Axtell et al. teaches a fluid ejection device, wherein the first transistor and the third transistor share the first active region (figure 7, elements 111 and 115).

As per claim 17, Axtell et al. teaches a fluid ejection device, wherein the first transistor and the second transistor share a second active region (figure 7, elements 111 and 113).

As per claim 18, Axtell et al. teaches a fluid ejection device, wherein the first transistor and the third transistor share a second active region (figure 7, elements 111 and 115).

As per claim 24, Axtell et al. teaches a device, comprising: a substrate having a first active region and a second active region (figure 7); a first gate (figure 7, element 105) configured in a first loop structure around the first active region; a second gate (figure 7, element 111) configured in a second loop structure around the second active region; and a third gate (figure 7, element 113) configured in a third loop structure around the first gate and the second gate.

As per claim 25, Axtell et al. teaches a device, wherein the first active region is isolated from the second gate and the second active region is isolated from the first gate (figure 7, elements 105 and 111).

As per claim 26, Axtell et al. teaches a device, wherein the substrate has a third active region and the third gate (figure 7, element 113) is disposed around the third

active region, wherein the third active region is in contact with the first gate and the second gate (figure 7, element 105 and 111).

As per claim 33, Axtell et al. teaches a device, comprising: a substrate having a first active region, a second active region and a third active region (figure 7); a first gate configured in a first loop structure around the first active region figure 7, element 111); a second gate configured in a second loop structure around the second active region (figure 7, element 113); and a third gate configured in a third loop structure around the third active region (figure 7, element 115), wherein the second active region is electrically coupled to the third active region.

As per claim 34, Axtell et al. teaches a device, wherein the first gate (figure 7, element 111) is disposed around the second gate (figure 7, element 113).

As per claim 35, Axtell et al. teaches a device, wherein the substrate has a fourth active region and comprising: a fourth gate configured in a fourth loop structure around the fourth active region, wherein the first gate is disposed around the second gate and the third gate is disposed around the fourth gate (figure 7, element 105).

As per claim 36, Axtell et al. teaches a device comprising: a first transistor having a first gate, a first active region and a second active region (figure 6, element 102), wherein the first gate is configured in a first loop structure around the first active region; and a second transistor (figure 6, element 104) having a second gate configured in a second loop structure around the second active region, wherein the second active

region and the first gate are configured to receive a first signal and the first active region is configured to provide a second signal in response to the first signal.

As per claim 36, Axtell et al. teaches a device, wherein the first active region is configured to provide a lower capacitance than the second active region. [0048].

As per claim 38, Axtell et al. teaches a method of controlling fluid ejection from a fluid ejection device, the method comprising: receiving energy pulses (figure 7, element 101); controlling a drive switch with a first transistor (figure 7, element 111) having a first gate configured in a first loop structure, a second transistor (figure 7, element 113) having a second gate configured in a second loop structure, and a third transistor (figure 7, element 115) having a third gate configured in a third loop structure disposed around the first transistor, wherein the second transistor and the third transistor share a first active region; and controlling, with the drive switch, the energy pulses to eject fluid [0048].

As per claim 39, Axtell et al. teaches a method further comprising: controlling the drive switch [0062] with a fourth transistor (figure 7, element 105) having a fourth gate configured in a fourth loop structure, wherein the second transistor and the fourth transistor (figure 7, elements 113 and 105) share a second active region and the first gate (figure 3, element 111) is disposed around a third active region that is electrically coupled to the second active region.

As per claim 40, Axtell et al. teaches a method further comprising: receiving, with a fourth active region, a signal to charge the second active region and the third active region, wherein the fourth gate is disposed around the fourth active region [0062].

As per claim 41, Axtell et al. teaches a method further comprising: controlling the drive switch [0062] with a fourth transistor having a fourth gate configured in a fourth loop structure, wherein the second transistor and the fourth transistor share a second active region (figure 7, element 113 and 105).

As per claim 42, Axtell et al. teaches a method, wherein the fourth gate (figure 7, element 105) is disposed around a third active region and the first gate (figure 7, element 111) is disposed around a fourth active region that is electrically coupled to the third active region.

As per claim 43, Axtell et al. teaches a method, wherein the third gate (figure 7, element 115) is disposed around the second transistor (figure 7, element 113).

As per claim 44, Axtell et al. teaches a method, wherein the first transistor and the second transistor share the first active region (figure 7, element 111 and 113).

Claims 19-21 and 27-31 are rejected under 35 U.S.C. 102(b) as being anticipated by Donahue et al. (US 6174037).

As per claim 19, Donahue et al. teaches a device comprising: a first transistor having a first gate configured in a first loop structure; a second transistor having a

second gate configured in a second loop structure; and a third transistor having a third gate configured in a third loop structure, wherein the first transistor and the second transistor are disposed within the third gate (figure 1, elements 68 – there are four in a row).

As per claim 20, Donahue et al. teaches a device, wherein the first transistor and the third transistor share an active region (figure 1, elements 68).

As per claim 21, Donahue et al. teaches a device, wherein the first transistor, the second transistor and the third transistor share an active region (figure 1, elements 68).

As per claim 27, Donahue et al. teaches a device comprising: a first transistor having a first gate configured in a first loop structure; a second transistor having a second gate configured in a second loop structure; a third transistor having a third gate configured in a third loop structure; and a fourth transistor having a fourth gate configured in a fourth loop structure (figure 2, elements 68 – there are four transistors), wherein the first transistor is disposed within the second gate and the third transistor is disposed within the fourth gate.

As per claim 28, Donahue et al. teaches a device, wherein the second transistor and the fourth transistor share an active region (figure 2, elements 68).

As per claim 29, Donahue et al. teaches a device, wherein the first gate is disposed around a first active region and the fourth gate is disposed around a second active region that is electrically coupled to the first active region (figure 2, elements 68).

As per claim 30, Donahue et al. teaches a device, wherein the third gate is disposed around a third active region configured to receive a signal to charge the first active region and the second active region (figure 2, elements 68).

As per claim 31, Donahue et al. teaches a device, wherein the first gate is disposed around a first active region and the third gate is disposed around a second active region that is electrically coupled to the first active region (figure 2, elements 68).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Axtell et al. (US 20020093551) in view of Matsumoto et al. (US 5057855).

Axtell et al. teaches a fluid ejection device; however, it does not teach a guard transistor.

Matsumoto et al. teaches a guard transistor (column 6, lines 44-56).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the fluid ejection device of Axtell et al. with the disclosure of Matsumoto et al. in order to guard the energy pulses within the cell.

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Axtell et al. (US 20020093551) in view of Donahue et al. (US 6174037).

As per claim 9, Axtell et al. teaches a fluid ejection device; however, it does not teach a fourth transistor having a fourth gate configured in a fourth loop structure, wherein the second gate is disposed around the fourth transistor.

Donahue et al. teaches a fourth transistor having a fourth gate configured in a fourth loop structure (figure 2, element 68), wherein the second gate is disposed around the fourth transistor.

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the fluid ejection device of Axtell et al. with the disclosure of Donahue et al. in order to create a more efficient electrical device.

Claims 22, 23, and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Donahue et al. (US 6174037) in view of Axtell et al. (US 20020093551).

Donahue et al. teaches a device.

As per claim 22, Donahue et al. does not teach a first transistor, a second transistor, and a third transistor sharing the first active region and the first gate is disposed around the second active region that is configured to receive a signal to change the first active region.

As per claim 23, Donahue et al. does not teach a drive switch, wherein the first transistor, second transistor, and third transistor share a first active region that is coupled to the drive switch and the first gate is disposed around a second active region that is coupled to data/address transistors.

As per claim 32, Donahue et al. does not teach a fourth gate disposed around a third active region configured to receive a signal to charge the first active region and the second active region.

As per claim 22, Axtell et al. teaches a first transistor, a second transistor, and a third transistor (figure 7, elements 111, 113, and 115) sharing the first active region and the first gate is disposed around the second active region that is configured to receive a signal to change the first active region [0062].

As per claim 23, Axtell et al. teaches a drive switch (figure 7, element 101), wherein the first transistor (figure 7, element 111), second transistor (figure 7, element 113), and third transistor (figure 7, element 115) share a first active region that is coupled to the drive switch and the first gate is disposed around a second active region that is coupled to data/address transistors (figure 7, elements 111 and 113).

As per claim 32, Axtell et al. teaches a fourth gate disposed around a third active region configured to receive a signal to charge the first active region and the second active region [0062].

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the device of Donahue et al. with the disclosure of Axtell et al. in order to create a more efficient electrical apparatus.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Laura E. Martin whose telephone number is (571) 272-2160. The examiner can normally be reached on Monday - Friday, 7:00 - 3:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen D. Meier can be reached on (571) 272-2149. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Laura E. Martin

5/1/06

MANISH S. SHAH
PRIMARY EXAMINER